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For

A Fabrication Method for a Device for Regulating Flow of Electric Current with High Dielectric Constant Gate Insulating Layer and Source/Drain Forming Schottky Contact or Schottky-like Region with Substrate

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A Fabrication Method for a Device for Regulating Flow of Electric Current with High Dielectric Constant Gate Insulating Layer and Source/Drain Forming Schottky Contact or Schottky-like Region with Substrate

BACKGROUND

The present invention is directed to fabrication methods for devices that regulate the flow of electric current.

An electric current flow regulating device such as semiconductor device 100 (for example a transistor), seen in prior art FIG. 1, may include a silicon substrate 110, with an impurity doped source 120 and impurity doped drain 130. Source 120 and drain 130 are separated by a channel region 140. Atop the channel region 140 is an insulating layer 150. Insulating layer 150 typically consists of silicon dioxide, which has a dielectric constant of 3.9. A gate electrode 160, made from electrically conductive material, is located on top of the insulating layer 150.

When a voltage V_G is applied to the gate electrode 160, current flows between the source 120 and drain 130 through the channel region 140. This current is referred to as the drive current, or I_D. For digital applications, a voltage V_G can be applied to the gate electrode 160, to turn the semiconductor device 100 "on." In this state, the semiconductor device will have a relatively large drive current, ideally limited only by the resistance of the channel region 140. A different voltage V_G can be applied to the gate electrode 160 to turn the semiconductor device 100 "off." In this state, the ideal leakage current is zero. However, in practical applications, the drive current in the "on" state is not ideal because of parasitic impedances associated with other parts of the semiconductor device 100. For example, the source and drain regions have a finite impedance, resulting in a parasitic impedance which adds to the resistance of the channel region. Also, in practical applications, there is a certain finite amount of leakage current when the semiconductor device is "off."

In prior art current regulating devices, the drive current is linearly proportional to the dielectric constant K of the insulating layer 150, and linearly inversely proportional to the thickness T_{ins} of the insulating layer 150. The drive current I_D is approximated by the relationship:

$$I_D \sim K/T_{ins}$$

where K is the dielectric constant of the insulating layer and T_{ins} is the thickness of the insulating layer.

One consideration in the design of current regulating devices is reducing the amount of power required to achieve a desired drive current. One way to reduce power consumption is by using a metal source and drain and a simple, uniformly implanted channel dopant profile, as described in copending U.S. Patent Applications 09/465,357, filed on December 16, 1999, entitled "METHOD OF MANUFACTURING A SHORT-CHANNEL FET WITH SCHOTTKY BARRIER SOURCE AND DRAIN CONTACTS," and 09/777,536, filed on February 6, 2001, entitled "MOSFET DEVICE AND MANUFACTURING METHOD," the contents of which are hereby incorporated by reference.

SUMMARY

By using the invention disclosed herein the drive current characteristics can be improved, resulting in a non-linear relationship between the drive current I_D and both the dielectric constant of the insulating layer, K, and the thickness of the insulating layer T_{ins}. The resulting relationship results in higher drive currents for larger K but constant K/T_{ins} ratios.

In one aspect, the invention provides a method for manufacturing a device for regulating the flow of electrical current. The method includes the steps of providing for a semiconductor substrate; providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0; providing for a gate electrode in contact with at least a portion of the insulating layer; and providing a source electrode and a drain electrode in contact with the semiconductor substrate and proximal to the gate electrode wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate. In one aspect, the device for regulating the flow of electrical current may be a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device. In another aspect, the dielectric constant may be greater than 7.6 or greater than 15.

In another aspect, the source and drain electrodes may be formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide. In another aspect, the source and drain electrodes may be formed from a member of the group

consisting of the rare earth silicides. In another aspect, the insulating layer may be formed from a member of the group consisting of the metal oxides. In another aspect, the Schottky contact or Schottky-like region may be at least in areas adjacent to the channel. In another aspect, an entire interface between at least one of the source and the drain electrodes and the semiconductor substrate may form a Schottky contact or Schottky-like region with the semiconductor substrate. In another aspect, the channel region may be doped.

In another aspect, the invention provides a method for manufacturing a device for regulating the flow of electrical current. The method includes the steps of providing for a semiconductor substrate; providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0; providing for a gate electrode located in contact with at least a portion of the insulating layer; exposing the semiconductor substrate on one or more areas proximal to the gate electrode; providing for a thin film of metal on at least a portion of the exposed semiconductor substrate; and reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and a drain electrode are formed on the semiconductor substrate. In one aspect, the device for regulating the flow of electrical current may be a MOSFET device. In another aspect, the dielectric constant may be greater than 7.6 or greater than 15.

In another aspect, the gate electrode may be provided by the steps of depositing a thin conducting film on the insulating layer; patterning and etching the conducting film to form a gate electrode; and forming one or more thin insulating layers on one or more sidewalls of the gate electrode. In another aspect, the method may include the step of removing metal not reacted during the reacting process. In another aspect, the reacting may include thermal annealing. In another aspect, the source and drain electrodes may be formed from a member of the group consisting of: platinum silicide, palladium silicide and iridium silicide. In another aspect, the source and drain electrodes may be formed from a member of the group consisting of the rare earth silicides. In another aspect, the insulating layer may be formed from a member of the group consisting of metal oxides. In another aspect, the Schottky contact or Schottky-like region may be formed at least in areas adjacent to the channel. In another aspect, an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate may form a Schottky contact or Schottky-like

region with the semiconductor substrate. In another aspect, dopants may be introduced into the channel region.

Aspects of the invention can include one or more of the following advantages. Conventional field effect transistors (FET) and other current regulating devices require a higher voltage than those fabricated in accordance with the invention to produce a similar drive current from source to drain. In an optimized conventional FET or current regulating device, the drive current varies generally linearly with the ratio of the insulating layer's dielectric constant to its thickness. One of the advantages of the invention is the unexpected result of the drive current being more sensitive to dielectric constant K than to T_{ins}, implying larger drive current I_d for larger K and constant K/T_{ins} ratio. These results are achieved by coupling a Schottky or Schottky-like source and/or drain with an insulating layer made of a high dielectric constant material. Lower voltage is required to produce high source to drain currents which results in lower power consumption for microelectronics utilizing this architecture.

Furthermore, the well-known benefit of achieving less gate leakage current (between gate and source/drain electrodes) by using larger K and constant K/T_{ins} ratio, will still be observed in the present invention. For conventionally architected devices this particular benefit is the sole reason for using high K materials for the gate insulator. No other significant benefit is expected or observed. By using Schottky or Schottky-like source/drain devices in combination with a larger K, an unexpected and dramatic improvement in drive current I_d is achieved in addition to the reduction in gate leakage current.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a cross-section of a prior art semiconductor transistor.

FIG. 2 is a cross-section of a semiconductor substrate with Schottky contact source and drain combined with a non-silicon dioxide insulating layer between the gate and channel region.

FIG. 3a is a cross-section of a semiconductor device with Schottky contact source and drain combined with a non-silicon dioxide insulating layer between the gate and channel region. This is the device structure used for numerical simulations.

FIG. 3b is a logarithmic plot showing the simulated relationship between the drive current I_D and gate voltage V_G for various K values, with the ratio K/T_{ins} held constant.

FIG. 3c is a linear plot with the same data as FIG. 3b.

FIG. 4 is a cross-section of semiconductor substrate after ion implantation.

FIG. 5 is a cross-section of semiconductor substrate after insulating layer growth and gate patterning.

FIG. 6 is a cross-section of semiconductor substrate after growth of an oxide layer on the sidewalls.

FIG. 7 is a cross-section of semiconductor substrate after creation of a metal silicide source and drain.

FIG. 8 is a cross-section of the semiconductor substrate resulting from the process steps outlined in FIG. 9.

FIG. 9 is a flow chart outlining the process flow for the fabrication of a device for regulating flow of electric current in accordance with the invention.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Referring to FIG. 2, semiconductor device 200 includes a substrate 210 in which a source 220 and drain 230 are formed. Substrate 210 may be composed of silicon or may be a silicon-on-insulator (SOI) substrate. Source 220 and/or drain 230 may be composed partially or fully of a rare earth silicide. Source 220 and/or drain 230 may also be composed partially or fully of platinum silicide, palladium silicide or iridium silicide. Because the source and drain are composed in part of a metal, they form Schottky contacts or Schottky-like regions 270, 275 with the substrate 210, where a "Schottky contact" is defined by the contact between a metal and a semiconductor, and a "Schottky-like region" is a region formed by the close proximity of a semiconductor and a metal. The Schottky contacts or Schottky-like regions 270, 275 can be formed by forming the source and/or drain from a metal silicide. The Schottky contacts or Schottky-like regions 270, 275 are in an area adjacent to a channel

region 240 formed between the source 220 and drain 230. The entire interface between either or both of the source 220 and the drain 230 may form a Schottky contact or Schottky-like region 270, 275 with the substrate 210. The channel region 240 may be impurity doped where the doping may be conventional non-uniform doping or may be uniform doping as described in copending U.S. Patent Application No. 09/465,357 and U.S. Patent Application No. 09/777,536.

An insulating layer 250 is formed on top of the channel region 240 and may be formed on part or all of the source 220 and drain 230. The insulating layer 250 is composed of a material with a dielectric constant greater than that of silicon dioxide; e.g. a dielectric constant greater than 3.9. For example, insulating layer 250 may be composed of a metal oxide such as TaO_2 with a dielectric constant of approximately 25, TiO_2 with a dielectric constant of approximately 50-60, HfO_2 with a dialectic constant of approximately 15-20, or ZrO_2 with a dielectric constant of approximately 15-20. The insulating layer 250 may consist of a dielectric with a modest K value (e.g., 5-10), such as nitride/oxide or oxy-nitride stack; a medium K value (e.g., 10-20), such as unary oxides Ta_2O_3, TiO_2, ZrO_2, HfO_2, Y_2O_3, La_2O_3, Gd_2O_3, Sc_2O_3 or silicates $ZrSiO_4$, $HfSiO_4$, $LaSiO_4$, or $TiSiO_4$; or a high K value (e.g., greater than 20) such as amorphous $LaAlO_3$, $ZrTiO_4$, $SnTiO_4$, or $SrZrO_4$, or single crystals $LaAl_3O_4$, $BaZrO_3$, Y_2O_3, La_2O_3. Optionally, to improve manufacturability issues associated with transition metals, the insulating layer 250 may consist of more than one layer. The insulating layer 250 may be formed with a "bi-layer" approach and may consist of more than one type of dielectric, e.g., TiO_2 on top of Si_3N_4. A gate electrode 260 is positioned on top of the insulating layer 250. A thin insulating layer 225 surrounds the gate electrode 260.

By forming a semiconductor device with (1) a source 220 or drain 230 forming a Schottky contact or Schottky-like region 270, 275 with the substrate 110; and (2) an insulating layer 250 with a relatively high dielectric constant, one is able to achieve a larger drive current I_d for larger K, but constant K/T_{ins}.

Referring to FIGs. 3a-c, full two dimensional electrostatic simulations were performed on the semiconductor device 305 structure of Figure 3a, for various insulating layer 309 thicknesses T_{ins} 307 and insulator dielectric constants K. The simulation assumes the following:

1) P type MOS semiconductor device 305, metallic source 301/drain 303 at 300K.

2) Metallic source 301/drain 303 with radius of curvature R 311 of 10nm.

3) Channel length L 313 of 25nm, drain voltage V_D of 1.2V.

4) No significant charge, either fixed or mobile, in the silicon substrate 315.

5) The drain current, I_D, is limited solely by the emission process at the source 301 end of the semiconductor device 305.

6) The current density versus electric field (J vs. E) characteristic for the emission process at the source 301 is modeled after a platinum silicide-to-silicon Schottky contact. The Schottky barrier height is assumed to be 0.187eV, hole effective mass in the silicon is $0.66m_o$, fermi level is at 5.4eV, and temperature is 300K. For a given electric field strength at a particular point on the source 301, the current density is calculated via a complete, no approximations solution to the Schröedinger equation assuming a 1-D sharp triangular barrier. The effects of quantum tunneling and reflection have been fully included. Because the total current density is integrated across the density of states, currents due to field emission, thermal emission, and thermally assisted field emission have been accounted for. The J vs. E relationship has been calibrated to experimental data for the pure thermal emission case (E=0).

These assumptions are valid in the real world case of short channel (<25nm) and undoped (or lightly doped) substrates. Although the absolute values of the calculated source 301 emission currents have not been calibrated for E>0, they are based on some experimental data and first-principles calculations. For the purposes of the proposed invention, the calculated J vs. E data is sufficient as the primary interest relates to the effect of the insulating layer 309 thickness (T_{ins}) 307 and dielectric constant (K) on source 301 emission current. Relative changes in source 301 emission current with T_{ins} and K are more relevant, in this case, than the absolute value of the current. Nevertheless, calculated values of both leakage and drive currents I_D are in good agreement with the measured data of actual transistors.

Simulations were run with a constant K/T_{ins} ratio of 0.156. The results are shown in FIGs. 3b-c. Starting with FIG. 3c, working upwards, curve 350 shows the relationship between the gate voltage V_G and the drive current I_D in a semiconductor device with an

insulating layer dielectric constant of 3.9 (T_{ins} = 25 Å). Curves 360, 370 and 380 show the ratio of V_G and I_D in semiconductor devices with sources 220 and drains 230 that form a Schottky contact or Schottky-like region 270, 275 with the substrate and insulating dielectric constants of 10 (T_{ins} = 64.1 Å), 25 (T_{ins} = 160.3 Å), and 50 (T_{ins} = 320.5 Å), respectively. Referring to FIG. 3b, curve 355 shows the logarithmic relationship between the gate voltage V_G and the drive current I_D in a semiconductor device with an insulating layer dielectric constant of 3.9 (T_{ins} = 25 Å). Curves 365, 375 and 385 show the logarithmic ratio of V_G and I_D in semiconductor devices with sources 220 and drains 230 that form a Schottky contact or Schottky-like region 270, 275 with the substrate and insulating dielectric constants of 10 (T_{ins} = 64.1 Å), 25 (T_{ins} = 160.3 Å), and 50 (T_{ins} = 320.5 Å), respectively. It is expected that similar results would be achieved regardless of the radius of curvature R 311, channel length 313 and drain voltage V_D. Drive current to leakage current ratios are 35, 38, 53 and 86 for the curves 350/355, 360/365, 370/375 and 380/385, respectively. Leakage currents can be lowered by at least a factor of 10, without sacrificing drive currents, by the addition of the appropriate dopants in the substrate (to control bulk-punchthrough currents) or by a reduction in operating temperature. Thus, by using a source 301 or drain 303 that forms a Schottky contact or Schottky-like region with the substrate, and by increasing K while maintaining a constant K/T_{ins} ratio, the drive current I_D increases significantly (from a little over 300 μA/μm for a V_G of 1.2V to approximately 1300 μA/μm). Thus, for a desired drive current, a device would need a significantly lower voltage to operate than that required by the prior art. Because power consumption varies with the square of the voltage, the invention provides for significantly lower power usage.

The device for regulating flow of electric current described above, for example a planar P-type or N-type MOSFET, may be formed using the process shown in FIGs. 4-8 and described in FIG. 9. (Note that the planar P-type or N-type MOSFET need not be planar in the horizontal direction, but may assume any planar orientation.) Referring to FIGs. 4 and 9, a thin screen oxide 323 is grown on silicon substrate 310, the substrate 310 having a means for electrically isolating transistors from one another (905). The thin screen oxide, optionally a thickness of 200 Å, acts as the implant mask for the channel region 340 doping. The appropriate channel dopant species (for example Arsenic and Indium for P-type and N-type

devices respectively) is then ion-implanted through the screen oxide 323 to a pre-determined depth in the silicon (for example, 1000 Å) (910).

Referring to FIGs. 5 and 9, the screen oxide layer 323 of FIG. 4 is removed with hydro-fluoric acid (915), and the thin insulating layer 450 is either grown or deposited at least on a portion of the channel region 340 (920). This insulating layer 450 may consist of TiO_2, TaO_2, or any other appropriate compound with a high dielectric constant as discussed above. Immediately following the insulating layer growth or deposition, an in-situ heavily doped silicon film is deposited (930). This silicon film will eventually make up the gate electrode 460. The silicon film may be doped with phosphorus for an N-type device or boron for a P-type device. The gate electrode 460 is then patterned with a lithographic technique and silicon etch that is highly selective to the insulating layer 450 (935).

Referring to FIGs. 6 and 9, a thin oxide, optionally approximately 100 Å in thickness, is formed on the top surface and sidewalls of the gate electrode 460 (940). Some of the oxide layers then are removed by anisotropic etch to expose the silicon on the horizontal surfaces 510, while preserving it on the vertical surfaces (945). This step serves both to create a gate sidewall oxide 525 and to electrically activate the dopants in the gate electrode 460 and channel region 340 of the device.

Referring to FIGs. 7 and 9, a metal is deposited as a blanket film, optionally approximately 400 Å thick, on all surfaces (950). The particular metal deposited will depend on whether the device is N-type or P-type. Platinum may be used for the P-type device while erbium may be used for an N-type device. The semiconductor device 600 is then annealed for a specified time at a specified temperature, for example, 45 minutes at 400C (955). Where the metal is in direct contact with the silicon, the annealing process causes a chemical reaction that converts the metal to a metal silicide 606. The metal 616 not in contact with silicon does not react.

Referring to FIGs. 8 and 9, the unreacted metal 616 is removed with a wet chemical etch (960). For example, if the deposited metal was platinum or erbium, aqua regia or HNO_3, respectively, may be used to remove it. The silicide electrodes that remain are the source 620 and drain 630. The Schottky device for regulating flow of electric current with a high dielectric constant insulating layer is now complete and ready for electrical contacting to gate electrode 460, source 620, and drain 630 (965).

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, the semiconductor devices illustrated in the claims are by way of example only. It should be understood that the concepts of the invention apply to semiconductor devices with a variety of cross-sections. And, although the invention has been illustrated with respect to planer silicon MOS transistors, it can apply equally well to other devices for regulating the flow of electrical current. For example, devices built on other semiconductor substrates such as gallium arsenide GaAs, indium phosphide InP, silicon carbide SiC, silicon germanium SiGe, etc. And, the invention is not limited to any particular ratio(s) of K/T_{ins}. Accordingly, other embodiments are within the scope of the following claims.